EXPEDITED PROCEDURE - EXAMINING GROUP 2831

S/N 09/537,274

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Larry Eugene Mosley	Examiner:	Eric W. Thomas
Serial No.:	09/537,274	Group Art Unit:	2831
Filed:	March 29, 2000	Docket:	884.240US1
Title:	MULTI-LAYER CHIP CAPACITOR		

AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116

Box RCE
Commissioner for Patents
Washington, D.C. 20231

In response to the final Office Action mailed November 7, 2001, please amend the application as follows:

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 1, 2, 9, 11, 14, 15, and 19. The specific amendments to individual claims are detailed in the following marked up set of claims.

1. (Twice Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductor layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductor layers.